Programmable Gate Array (FPGA) and Application Specific Logic Areas (ASLA) and the interconnections used (See Office Action paper number 12 at paragraph 7). Additionally, the Examiner asserts that Figs. 3-5 of '202 disclose interface architecture that is either mask-defined or FPGA programmable, comprising an FPGA portion of said integrated circuit having logic blocks ... and interconnect conductors for programmable connections. The Examiner further asserts that '202 discloses a mask-defined ASLA. The Examiner asserts that '202 discloses mask-defined routing for interconnecting FPGA and ASLA. Applicants respectfully disagree with the Examiner's assertions.

To anticipate a claim under 35 U.S.C. § 102, a single source must contain all of the elements of the claim. *Lewmar Marine Inc. v. Barient, Inc.*, 827 F.2d 744, 747, 3 U.S.P.Q.2d 1766, 1768 (Fed. Cir. 1987), *cert. denied*, 484 U.S. 1007 (1988).

Moreover, the single source must disclose all of the claimed elements "arranged as in the claim." *Structural Rubber Prods. Co. v. Park Rubber Co.*, 749 F.2d 707, 716, 223 U.S.P.Q. 1264, 1271 (Fed. Cir. 1984).

'202 merely discloses the combining of FPGA and ASLA by selectively interconnected programmable switch matrices (Col. 3, and lines 48-62). A monolithic IC having FPGA and mask-defined gate array portions wherein on-chip interconnection combines field programmable routing and mask-defined routing to interconnect such portions to each other and to I/O pads (Col. 4, lines 15-20). These routing to interconnects are further defined by '202 as the routing signals from one configurable logic block (CLB) to other CLBs, or between CLBs and mask-defined routing or programmable routing, by switch matrices. The switch matrices can selectively connect any routing signal to any other routing signal connected to its input/output terminals (Col. 5, lines 44-55). The special long lines are for special signals that extend across several columns of the local interconnect lines on the FPGA (Col. 6, lines 34-44). The routing to interconnect is defined as using switch matrices for routing signals to the CLB. Fig 6 illustrates the use of special long lines for special signals ... these long lines are mask-defined in the preferred embodiment. Furthermore, as shown in Fig. 7, connection from switch matrices to the long lines may be selectively implemented... (Col. 6, lines 34-44). These long lines are connected to the switch matrices for routing of signals to the CLBs and never bypassing the switch routing. This falls short of the claimed invention.

In contrast, the present invention cites in Claim 1, "mask programmed dedicated interface tracks connected between said logic blocks in said FPGA portion and said mask programmed interconnect conductors in said Application Specific Integrated Circuit (ASIC) portion". '202 does not disclose mask programmed dedicated interface tracks connected between said logic blocks in said FPGA portion and said mask programmed interconnect conductors in said ASIC portion. Therefore, '202 does not disclose each and every claimed element.

Since '202 fails to claim each and every element of the present invention, '202 does not anticipate the present invention.

The argument set forth above is equally applicable to dependent Claims 2, 3, 7-9 and 11-19. Independent Claim 1 being allowable, the dependent claims must also be allowable.

Applicants respectfully request that the rejection be withdrawn.

In view of the foregoing, it is respectfully asserted that Claims 1-20 are now in condition for allowance.

The 35 U.S.C. § 103 Rejection

Claims 4-6 stand rejected under 35 U.S.C. § 103 as being allegedly unpatentable over '202 in view of Bertolet et al., (U.S. Patent No. 5,671,432, hereinafter "'432"). Claim 10 stands rejected under 35 U.S.C. § 103 as being allegedly unpatentable over '202 in view of Sharma et al., (U.S. Patent No. 5,878,051, hereinafter "'051"), Berttolet and Bocchino, (U.S. Patent 5,869,979, hereinafter "'979"). Claims 16-19 stand rejected under 35 U.S.C. § 103 as being allegedly unpatentable over '202 Claim 20 stands rejected under 35 U.S.C. § 103 as being allegedly unpatentable over '202 in view of Aggarwal paper, 'Routing Architectures for Hierarchical field Programmable Gate Arrays' (hereinafter "Aggarwal paper") and Rush (U.S. Patent No. 5,742,181, hereinafter "'181"). This rejection is respectfully traversed.

The Examiner does not assert that Claim 1 is obvious in view of any references. Therefore, Claim 1 is nonobvious.

In addition, the cited references do not render Claim 1 obvious either.

To establish a *prima facie* case of obviousness, three basic criteria must be met. There must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the fences or to combine the references' teachings. There must be a reasonable expectation of success. Finally, the prior art references must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in the applicant's disclosure. *In re Vaeck*, 20 USPQ2nd 1438 (Fed. Cir. 1991).

In order to render claims *prima facie* obvious, each and every claimed element must be taught or suggested in the prior art references.

Claim 1 claims in part, "mask programmed dedicated interface tracks connected between said logic blocks in said FPGA portion and said mask programmed interconnect conductors in said ASIC portion".

'202 in view of '432, '051, '979, Aggarwal paper, and '181 does not teach or suggest mask programmed dedicated interface tracks connected between said logic blocks in said FPGA portion and said mask programmed interconnect conductors in said ASIC portion. Therefore, the cited references, '202 in view of '432, '051, '979, Aggarwal paper, and '181, do not teach or suggest all of the claimed elements.

Since '202 in view of '432, '051, '979, Aggarwal paper, and '181 fails to teach or suggest all of the claimed elements, then '202 in view '432, '051, '979, Aggarwal paper, and '181 do not make a *prima facie* case of obviousness.

If an independent claim is nonobvious under 35 U.S.C. § 103, then any claim depending therefrom is nonobvious. *In re Fine*, 837 F.2d 1071, 5 U.S.P.Q. 2d 1596 (Fed. Cir. 1988).

Dependent Claims 2-20

Claims 2-20 are dependent on independent Claim 1. Claim 1 being nonobvious, dependent Claims 2-20 are also nonobvious.

Applicants respectfully request that the obviousness rejection of Claims 4-6, 10, 16-19, and 20 be withdrawn.

In view of the foregoing, it is respectfully asserted that Claims 1-20 are now in condition for allowance.

Claims 21-23, 27-29, and 31-36

Claims 21-23, 27-29, and 31-36 stand rejected under 35 U.S.C. § 103 as being allegedly unpatentable over '202 in view of '432, '051, '979, Aggarwal paper, and '181. This rejection is respectfully traversed.

The Examiner asserts that '202 discloses an integrated circuit with field programmable and application specific logic areas (ASLA) and the interconnections used (See Office Action paper number 12 at paragraph 14). Additionally, the Examiner asserts that '202 does not teach hierarchical design structures. Applicants agree. The Examiner asserts that the Aggarwal paper discloses routing architectures for hierarchical Field Programmable Gate Arrays (FPGAs). The Examiner further asserts that '181 discloses FPGAs with hierarchical interconnect structures. The Examiner concludes that it would have been obvious to one of ordinary skill in the art at the time of the invention to modify '202 with the Aggarwal paper and '181 and implement a hierarchical FPGA having the advantages of lower density and increased routing efficiency.

Additionally, the Examiner asserts that Figs. 3-5 of '202 disclose interface architecture that is either mask-defined or FPGA programmable. The Examiner further asserts that the Aggarwal paper teaches FPGA hierarchical designs (pp.475-477). The Examiner asserts that '181 teaches FPGAs or generally programmable atomic logic elements with a hierarchical interconnect structure. Further, the Examiner asserts that '202 discloses a mask-defined ALSA. The Examiner asserts that '202 discloses mask-defined routing for interconnecting FPGA and ASLA, therefore it is obvious. Applicants disagree with the assertions of the Examiner.

To establish a *prima facie* case of obviousness, three basic criteria must be met. There must be some suggestion or motivation, either in the references themselves or in the knowledge generally available in to one of ordinary skill in the art, to modify the fences or to combine the references' teachings. There must be a reasonable expectation of success. Finally, the prior art references must teach or suggest all the claim limitations.

The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in the applicant's disclosure. *In re Vaeck*, 20 USPQ2nd 1438 (Fed. Cir. 1991).

The Aggarwal paper teaches a hierarchical interconnect architecture. In a hierarchical architecture, the logic elements are organized in groups, or hierarchy levels, such that each group contains interconnect wires that support communication only within that group. Separate wires are provided to enable communication between the groups. A hierarchical interconnect architecture allows user circuit designs to be implanted using a mix of short and long wiring resources resulting in improved local interconnection. Communications are contained within the group (Aggarwal paper, pages 475-477).

'181 builds on the Aggarwal paper and teaches a hierarchical interconnect structure with local interconnectivity at the same time as long interconnections using fewer switches (Col. 4, line 10 to Col. 13, line 8). The hyperlink connection eliminates one switch from the signal path, reducing the total number of switches (Col. 7, lines 31-43). Special purpose interconnects may also be provided, however this carry system does not extend outside of any block. A block is a subset or small area with the larger FPGA (Col. 11, lines 31-54).

'202, as argued above, merely teaches the combining of FPGA and ASLA by selectively interconnected programmable switch matrices (Col. 3, lines 48-62). A monolithic IC having FPGA and mask-defined gate array portions wherein on-chip interconnection combines field programmable routing and mask-defined routing to interconnect such portions to each other and to I/O pads (Col. 4, lines 15-20). These routing to interconnects are further defined by '202 as the routing signals from one configurable logic block (CLB) to other CLBs, or between CLBs and mask-defined routing or programmable routing, by switch matrices. The switch matrices can selectively connect any routing signal to any other routing signal connected to its input/output terminals (Col. 5, lines 44-55). The special long lines are for special signals that extend across several columns of the local interconnect lines on the FPGA (Col. 6, lines 34-44). The routing to interconnect is defined as using switch matrices for routing signals to the CLBs. Fig 6 illustrates the use of special long lines for special signals ... these long lines are mask-defined in the preferred embodiment. Furthermore, as shown in Fig. 7, connection from switch matrices to the long lines may be selectively implemented ...(Col. 6, lines 34-44). These long lines are connected to the switch matrices for routing

of signals to the CLBs and never bypassing the switch routing. This falls short of the claimed invention.

In contrast the present invention cites in part in Claim 1, "mask programmed dedicated interface tracks connected between said logic blocks in said FPGA portion and said mask programmed interconnect conductors in said ASIC portion". '202 in view of the Aggarwal paper and '181 does not teach or suggest mask programmed dedicated interface tracks connected between said logic blocks in said FPGA portion and said mask programmed interconnect conductors in said ASIC portion. Therefore, '202 in view of Aggarwal paper and '181 does not teach or suggest all of the claimed elements.

Since '202 in view of '432, '051, '979, Aggarwal paper, and '181 fails to teach or suggest all of the claimed elements, then '202 in view of '432, '051, '979, Aggarwal paper, and '181 does not make a *prima facie* case of obviousness.

Additionally, obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. *In re Fine*, 5 USPQ2d 1596 (Fed. Dir. 1988).

A factor cutting against a finding of motivation to combine or modify the prior art is when the prior art teaches away from the claimed combination. A reference may be said to teach away when a person of ordinary skill, upon reading the reference, would be discouraged from following the path set out in the reference, or would be led in a direction divergent from the path that the applicant took. *In re Gurley*, 31 USPQ 2nd 1130 (Fed. Cir. 1994).

The teachings of '181 teach away from the teachings of '202. '181 teaches a hierarchical interconnect structure with local interconnectivity at the same time as long interconnections using fewer switches (Col. 4, line 10 to Col. 13, line 8). The hyperlink connection eliminates one switch from the signal path, reducing the number of switches (Col. 7, lines 31-43).

'181 teaches that the interconnect levels are 0-6 with each high level encompassing the lower level. In general, each hierarchical level in the interconnect

network supports electrical communication within subsections of an emulation system. These subsections are referred to as "leaves", "blocks", "sectors", "chips" and a "system". When communications is required outside of a particular subsection, an interconnection must be made using a higher level of the hierarchy (Col. 4, line 66 to Col. 5, line 24).

'181 teaches that a Programmable Atomic Logic Element (PALE) produces a data output signal distributed to multiple data output drivers in order to increase the number of hierarchical levels that are directly accessible to the output to the PALE (Col. 6, lines 17-26). The hierarchical structure is supplemented by a carry subsystem that provides special purpose interconnections (Col. 7, line 66 to Col. 8, line 1). The carry subsystem supplements the hierarchical interconnect structure for special purpose interconnects (Col. 11, lines 30-32). The carry signal can propagate through many PALEs in a leaf (Col. 11, lines 41-42). The carry system based on system efficiencies does not extend outside of any block (Col. 11, lines 52-53). '181 constrains the special purpose interconnects within any given block. A block is a subset or small area with the larger FPGA.

In contrast, the '202 reference teaches the combining of FPGA and ASLA with selectively interconnected programmable switch matrices (Col. 3, lines 48-62). '202 teaches special long lines for special signals extending across several columns of local interconnect lines of the FPGA (Col. 6, lines 34-44). These long lines may be driven by the ASLA, which is off chip from the FPGA, (Col. 6, lines 52-56). This interconnection by definition creates connections outside the '181 Block constraint.

'181 teaches a system that is constrained to local routing resources and lower levels of the hierarchical interconnected network. Therefore, '181 teaches away from '202 and away from the present invention.

'181 teaches by analogy, communications within a group of office buildings contained within one complex. Each individual office building has internal communication lines. When communicating outside the office building, all communications are routed from the nearest office building to the next nearest office building to the next nearest in a serial fashion until the destination office building is contacted. If one office building requires many contacts with a far office building without the delays of serial contacts, there can be special direct line for connection made. When an office building within one complex wants to communicate to an outside office

building in another complex, a long distance operator is used. '181 specifically disallows bypassing the long distance operator.

In contrast, Claim 1 of the present invention claims "mask programmed dedicated interface tracks connected between said logic blocks in said FPGA portion and said mask programmed interconnect conductors in said ASIC portion". '181 teaches away from mask programmed dedicated interface tracks connected between said logic blocks in said FPGA portion and said mask programmed interconnect conductors in said ASIC portion.

Therefore, '181 teaches away from the present claimed elements.

Since '181 teaches away from the present claimed elements, there is no motivation or suggestion to combine '181 with '202. Without any motivation or suggestion to combine '181 with '202, there is no *prima facie* case of obviousness.

Reconsideration and withdrawal of the rejection of Claim 21 under 35 U.S.C §103 is respectfully requested.

In view of the foregoing, it is respectfully asserted that Claim 21 is now in condition for allowance.

Dependent Claims 22-39

If an independent claim is nonobvious under 35 U.S.C. § 103, then any claim depending therefrom is nonobvious. *In re Fine*, 837 F.2d 1071, 5 U.S.P.Q. 2d 1596 (Fed. Cir. 1988).

Independent Claim 21 being allowable, dependent Claims 22-39 must also be allowable.

Reconsideration and withdrawal of the rejection of Claims 22-39 under 35 U.S.C §103 is respectfully requested.

In view of the foregoing, it is respectfully asserted that all Claims are now in condition for allowance.

Request for Entry of Amendment

It is believed that the forgoing places the above-identified patent application into condition for allowance. Early and favorable consideration of this Response is earnestly solicited.

If, in the opinion of the Examiner, an interview would expedite the prosecution of this application, the Examiner is invited to call the undersigned attorney at the number indicated below.

In the event the patent office charges a fee for filing the above-noted documents, including any fees required under 37 CFR 1.136 for any necessary Extension of Time to make the filing of the attached documents timely, the Assistant Commissioner is hereby authorized to charge or credit the difference to our Deposit Account No. 50-0612. An additional copy of this page is enclosed.

Respectfully submitted,
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Dated:

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